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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/901,936	Applicant(s) NOONBURG, DEREK B.	
	Examiner Joni Hsu	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 5, 2007 have been considered but are not persuasive.

2. As per Claim 1, Applicant argues Rege (US005390299A) has nothing to do with present invention. Present invention has to do with reducing bandwidth necessary to retrieve pixel data. Rege relates to communication interface adapter employing buffer memory in transfer of data packets between data network and host computer. Rege relates to minimizing packet loss that arises from buffer memory congestion in host network adapter, congestion control, and bringing back operation of network to stable point after it has reached severe overload and has potentially lost packets. These are completely different functions (p. 12).

In response to applicant's argument that references fail to show certain features of applicant's invention, it is noted that features upon which applicant relies (i.e., reducing bandwidth necessary to retrieve pixel data) are not recited in rejected claim(s). Although claims are interpreted in light of specification, limitations from specification are not read into claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner also points out according to Applicant's disclosure, present invention has to do with controlling amount of data in data packets transferred between buffer memory and peripherals [0015, 0016, 0018]. Rege teaches transferring data between buffer memory and peripherals in data packets (c. 1, ll. 15-29). Rege teaches avoiding receive-side buffer memory congestion, and so system monitors packet transfer to control amount of data in data packets transferred (c. 1, ll. 62-c. 2, ll. 2; c. 6, ll. 18-22). Therefore, Rege is considered to be related to the present invention.

3. Applicant argues "bandwidth," "packetizing," "packetization" or "combining" aren't in Rege. "Loss," "lost," "congestion," or "overload" aren't in Applicant's disclosure (p. 12-13).

First of all, Examiner points out that the word "bandwidth" does not appear in claims. Second of all, Examiner points out exact words Applicant uses do not necessarily have to be found in Rege. Rege can use words that have same meaning as words Applicant uses. Words do not have to be exactly the same. According to Applicant's disclosure, bandwidth is referred to as capacity of memory bus to transfer data packets between buffer memory and peripherals [0015]. Rege teaches transferring data between buffer memory and peripherals in data packets (c. 1, ll. 15-29). Rege teaches avoiding receive-side buffer memory congestion, and so system monitors packet transfer to ensure there is sufficient capacity to transfer data packets so buffers are not overflowed (c. 1, ll. 62-c. 2, ll. 20), and so ensures there is sufficient bandwidth. Rege teaches packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 18-22). So, Rege teaches storing packets in pages, and determining whether packets need to be divided among multiple pages or whether packet can be combined into one page, and this is considered to teach packetizing, packetization, or combining.

4. Applicant argues Artieri (US005579052A) and Rege do not share any common classes in received Fields of Search. So, Rege is not in same field as Artieri, or as present invention (p. 13).

In response to applicant's argument that Rege is nonanalogous art, it has been held that prior art reference must either be in field of applicant's endeavor or, if not, then be reasonably pertinent to particular problem with which applicant was concerned, in order to be relied upon as a basis for rejection of claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Rege, Artieri, and present invention all have to do with controlling

amount of data transferred in data packets (c. 1, ll. 62-68 in Rege; c. 3, ll. 34-51 in Artieri; [0018] in Applicant's disclosure). So, even though Rege and Artieri have different Fields of Search, they are reasonably pertinent to particular problem with which applicant was concerned, and so they are analogous art and can be used to reject claims.

5. Applicant argues while Rege does teach storing packets into plurality of "pages" of 512 bytes each and retrieving them, it does not teach packetizing data, i.e., creating packets (or altering data within them). Rege does not suggest buffer selects scheme for packetizing data. Buffer of Rege merely receives packets, stores them sequentially after breaking them into segments 512 bytes long, and then retrieves them sequentially. Thus, Examiner's statement "therefore the packetization scheme is selected based on how many pages of data need to be read" is false. To the contrary, it is previously selected packetization scheme that determines what data is in packet and thus how many pages of data need to be read, as number of pages follows directly from number of bytes in packet. Even if merely dividing packet into fixed length units could be characterized as "scheme," Rege does not teach selecting such scheme based upon locations of read data, but only based upon predefined length of pages in buffer (p. 13-14).

In reply, Examiner points out Rege teaches breaking packets into segments 512 bytes long (c. 6, ll. 18-22), and so Rege teaches altering data within packets, and so this is considered to be packetizing data. Rege teaches packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 18-22). So, packets are divided into portions that are equal to the size of pages, and so packetization scheme is selected based on how many pages of data need to be read. Since memory stores plurality of

pages (c. 6, ll. 14-18), this means each page has a location in memory. So, packetization scheme is selected based on locations of read data (c. 6, ll. 18-22).

6. Applicant argues Rege states each ring entry contains start of packet bit and end of packet bit. This indicates buffer of Rege is not selecting packetization scheme but merely taking packet in form in which it is delivered to buffer (p. 14). Both Artieri and Rege concern order in which packets are read from memory. This has nothing to do with how packets are created. In Rege data arrives already assembled into packets which are merely stored in segments of fixed size. Rege does not teach retrieving the data in any other fashion than that in which it is stored in buffer, but rather is limited to storing data in fixed length segments and sending data on in same packetized form in which it was received (p. 15).

In reply, Examiner points out the dividing of packets into portions that are equal to size of pages as taught in Rege (c. 6, ll. 18-22) is considered to be selecting a packetization scheme.

7. As per Claim 19, Applicant argues Rege fails to show packing selected portions of read data into data packets according to specifications of read command or sending instructions about how to retrieve data, but rather only shows entire received data packet may be broken into fixed length portions for storage in and retrieval from buffer. There is no modification of packet, no selecting of portions of data to be included, and no connection shown between packetization scheme and read command (page 16).

In reply, Rege teaches pool of pages 300 is array of pages 305, which are 512 bytes large, so packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 13-22). Since packet is divided into pages, this means packet is modified. Rege teaches if packet is large, portions of packet are selected to be

included in plurality of pages (c. 6, ll. 13-22), and so Rege teaches selecting of portions of data to be included. Packets are transmitted by adapter 103 reading packet from memory 102 and transmitting it over network bus 105. Within packet is address of destination node on network (c. 4, ll. 59-66). CPU 101 accesses adapter control and status registers to control and monitor operation of adapter 103 (c. 5, ll. 15-20), and CPU 101 can pass commands to adapter 103 (c. 5, ll. 29-39). So, CPU 101 sends read commands to adapter 103, and in response to read commands (c. 5, ll. 15-20, 29-39), adapter reads data from memory 102 and transmits it over network bus 104 to destination node on network (c. 4, ll. 59-66). Destination node receives packet through its adapter 103 (c. 4, ll. 67-c. 5, ll. 12). Adapter 103 receives packets (c. 5, ll. 1-4, 40-45) and stores packets in packet buffer memory 200 containing pool of pages 300. Pool of pages 300 is array of pages 305, which are 512 bytes large, so packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6; ll. 13-22). So, adapter 103 receives data read from memory 102 of source node (c. 4. ll. 67-c. 5, ll. 12) and packs read data received into data packets that are stored in packet buffer memory 200 of destination node (c. 5, ll. 40-45; c. 6, ll. 13-22). Since CPU 101 sends commands to adapter 103 to control adapter 103 (c. 5, ll. 14-20, 29-39), CPU 101 sends commands to adapter 103 including specifications on reading data from packet buffer memory 200 of source node (c. 7, ll. 36-39; c. 4, ll. 49-66) and how data is to be packed into data packets that are stored in packet buffer memory 200 of destination node (c. 4, ll. 49-68; c. 5, ll. 1-12, 14-20, 29-45; c. 6, ll. 13-22). So, Rege teaches connection between packetization scheme and read command.

8. As per Claim 28, Applicant argues Rege does not teach packing reference pixel data into data packets, but merely receiving data packets and storing them as words in plurality of memory

pages. Memory commands of Rege are merely commands to retrieve data from specified memory pages and link them together in sequence to recreate packets, and do not contain any "specifications" for packing data into packets as term is used in present invention (p. 19-20).

In reply, the Examiner points out that Artieri was used to teach this limitation.

Claim Rejections - 35 USC § 102

9. Text of sections of Title 35, U.S. Code 102(b) not included can be found in prior action.

10. Claims 1-3, 14, 15, 19, and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Rege (US005390299A).

11. As per Claim 1, Rege teaches generating memory requests to fetch read data from plurality of locations in memory (200, Fig. 2; c. 7, ll. 36-39), memory having plurality of memory pages (305, Fig. 3; c. 6, ll. 14-18) each of memory pages having plurality of words (c. 6, ll. 60-65), determining locations of read data in memory (c. 6, ll. 29-35, 57-59). Packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 18-22). So, Rege teaches storing packets in pages, and determining whether packets need to be divided among multiple pages or whether packet can be combined into one page, and this is considered to teach packetizing, packetization, or combining. Packets are divided into portions that are equal to the size of pages, and so packetization scheme is selected based on how many pages of data need to be read. Since memory stores plurality of pages (c. 6, ll. 14-18), this means that each page has location in memory. So, packetization scheme is selected based on locations of read data (c. 6, ll. 18-22). Rege teaches assembling at least one read command for addressing plurality of locations of read data; and fetching read data from memory locations and combining it into plurality of data packets in accordance with

selected packetization scheme, wherein at least one data packet contains data from more than one of plurality of memory pages (c. 6, ll. 12-48, 60-68; c. 7, ll. 1-12, 36-48). Rege teaches breaking packets into segments 512 bytes long (c. 6, ll. 18-22), and so Rege teaches altering data within packets, and so this is considered to be packetizing data. Dividing of packets into portions that are equal to size of pages (c. 6, ll. 18-22) is considered to be selecting packetization scheme.

12. As per Claim 2, Rege teaches step of sending at least one read command corresponding to plurality of data packets to memory (c. 4, ll. 59-65; c. 5, ll. 31-39).

13. As per Claim 3, Rege teaches step of fetching read data in response to sending at least one read command (c. 4, ll. 59-65; c. 5, ll. 31-39).

14. As per Claim 14, Rege teaches each of at least one read command includes specifications for combining selected ones of plurality of words from selected ones of plurality of memory pages into data packets (c. 6, ll. 18-22, 40-48, 60-63; c. 7, ll. 36-39; c. 4, ll. 59-65; c. 5, ll. 31-39).

15. As per Claim 15, Rege teaches if there are not enough pages available for subsequent packets, then subsequent packets are discarded (c. 10, ll. 18-23), which means plurality of packets cannot exceed predetermined number. So, plurality of data packets is equal to or less than predetermined number.

16. As per Claim 19, Rege teaches method for packing read data into data packets (c. 6, ll. 18-22), read data being stored in plurality of locations in memory (200, Fig. 2; c. 7, ll. 36-39), memory having plurality of memory pages (305, Fig. 3; c. 6, ll. 14-18). Packets are transmitted from one node 100 to another (c. 4, ll. 57-59). Each node 100 has CPU 101, host memory 102, and network adapter 103 (c. 4, ll. 44-46). Adapter 103 stores packets in host memory 102 by first storing packet data in packet buffer memory 200 (c. 5, ll. 40-45; c. 6, ll. 12-22), then reading

packet data from packet buffer memory 200 and writing it into host memory 102 (c. 7, ll. 36-39). Packets are transmitted by adapter 103 reading packet from memory 102 and transmitting it over network bus 105. Within packet is address of destination node on network (c. 4, ll. 59-66). CPU 101 accesses adapter control and status registers to control and monitor operation of adapter 103 (c. 5, ll. 15-20), and CPU 101 can pass commands to adapter 103 (c. 5, ll. 29-39). So, CPU 101 sends read commands to adapter 103, and in response to read commands (c. 5, ll. 15-20, 29-39), adapter reads data from memory 102 and transmits it over network bus 104 to destination node on network (c. 4, ll. 59-66). Destination node receives packet through its adapter 103 (c. 4, ll. 67-c. 5, ll. 12). Adapter 103 receives packets (c. 5, ll. 1-4, 40-45) and stores packets in packet buffer memory 200 containing pool of pages 300. Pool of pages 300 is array of pages 305, which are 512 bytes large, so packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 13-22). Since packet is divided into pages, this means packet is modified. Rege teaches if packet is large, portions of packet are selected to be included in plurality of pages (c. 6, ll. 13-22), and so Rege teaches selecting of portions of data to be included. So, adapter 103 receives data read from memory 102 of source node (c. 4. ll. 67-c. 5, ll. 12) and packs read data received into data packets that are stored in packet buffer memory 200 of destination node (c. 5, ll. 40-45; c. 6, ll. 13-22). Since CPU 101 sends commands to the adapter 103 to control adapter 103 (c. 5, ll. 14-20, 29-39), CPU 101 sends commands to adapter 103 including specifications on reading data from packet buffer memory 200 of source node (c. 7, ll. 36-39; c. 4, ll. 49-66) and how data is to be packed into data packets that are stored in packet buffer memory 200 of destination node (c. 4, ll. 49-68; c. 5, ll. 1-12, 14-20, 29-45; c. 6, ll. 13-22). So, method has steps of receiving at least one read command

requesting read data, at least one read command comprising specifications for including in data packets plurality of selected portions of read data from plurality of memory pages; sending instructions to memory (memory 102 of the source node 100) according to at least one read command received, instructions relating to manner in which read data requested is to be obtained from memory (c. 4, ll. 44-46, 49-66; c. 5, ll. 40-45; c. 6, ll. 12-22; c. 7, ll. 36-39); receiving read data from memory in response to memory receiving instructions; and packing read data received into data packets according to specifications of each of at least one read commands, wherein at least one data packet contains data form more than one of plurality of memory pages (c. 4, ll. 49-68; c. 5, ll. 1-12, 14-20, 29-45; c. 6, ll. 13-22).

17. As per Claims 24 and 26, Claims 24 and 26 are similar in scope to Claim 1, and therefore are rejected under the same rationale. As per Claims 25 and 27, Claims 25 and 27 are similar in scope to Claim 19, and therefore are rejected under the same rationale.

18. Thus, it reasonably appears that Rege describes or discloses every element of Claims 1-3, 14, 15, 19, and 24-27 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

19. Text of sections of Title 35, U.S. Code 103(a) not included can be found in prior action.

20. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A).

21. As per Claim 16, Rege teaches selected ones of plurality of memory pages is two (c. 6, ll. 18-22). Rege teaches predetermined threshold of pages, and detecting overflow when packet is discarded due to lack of free pages (c. 2, ll. 10-15). Rege does not explicitly teach predetermined

number is four. However, it would be obvious to adjust predetermined threshold of pages to any number, and so predetermined number of packets can be any number, and therefore can be four.

22. As per Claim 17, Rege teaches packets between 512 and 1024 bytes are stored in two pages 305, etc., meaning if size of packets is bigger, they can be stored in three pages. Rege teaches predetermined threshold of pages, and detecting overflow when packet is discarded due to lack of free pages (c. 2, ll. 10-15). Rege does not explicitly teach predetermined number is four. However, it would be obvious to adjust predetermined threshold of pages to any number, and so the predetermined number of packets can be any number, and therefore can be four.

23. Claims 4, 10, 11, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) in view of McGuinness (US006104416A).

24. As per Claim 4, Rege is relied upon for teachings as discussed above relative to Claim 1.

But, Rege does not specify what type of data is being read, and does not teach read data has reference pixel chunk having luminance chunk and chrominance chunk. But, McGuinness teaches read data has reference pixel chunk having luminance chunk and chrominance chunk (c. 4, ll. 40-52). Luminance chunks and chrominance chunks are stored in memory (c. 4, ll. 40-52). Arbitrary array portion of digital array is retrieved from memory. Word address corresponding to first datum of array portion is determined. Number of tiles that contain data in array portion is determined. Desired array portion is then read from memory by reading part of each tile in one memory burst (c. 3, ll. 36-42). So, addresses of luminance chunk and chrominance chunk data to be read in one memory burst are determined, and data is read from those addresses in one memory burst. So, data to be read in one memory burst is selected based on location of luminance chunk and chrominance chunk. Since Rege teaches selecting packetization scheme

based on location of data, method of Rege can be modified so data has luminance chunks and chrominance chunks, and data to be read in one memory burst for packet is selected based on location of luminance chunk and chrominance chunk, as suggested by McGuinness, and selecting data to be read for packet is considered to be selecting packetization scheme.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Rege's method of selecting packetization scheme so it is used for reading data having reference pixel chunk having luminance chunk and chrominance chunk because McGuinness teaches transmitting encoded bitstream for video is needed in many applications, such as watching television or using DVD player or computer (c. 1, ll. 48-53, 63-67; c. 2, ll. 1). Encoded bitstream for video includes reference pixel chunk having luminance chunk and chrominance chunk (c. 4, ll. 33-52). So, it would be advantageous to implement Rege's efficient method of transferring data by selecting packetization scheme (c. 1, ll. 10-13; c. 6, ll. 18-22, 60-68; c. 7, ll. 1-12, 36-48 in Rege) soit is used for reading data having reference pixel chunk having luminance chunk and chrominance chunk as suggested by McGuinness.

25. As per Claim 10, Rege does not teach placing virtual memory page boundary across luminance chunk, virtual memory page boundary being associated with packetization scheme. According to Applicant's disclosure, virtual page boundary is placed to split left 2 words of each row. So, chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create symmetry that allows reduction of number of cases that need to be considered for packetization [0068]. McGuinness teaches interlacing luminance Y and both chrominance Cr and Cb so all of the components can be retrieved in one word, reducing latency during rasterization without increasing time needed to

retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (c. 10, ll. 26-30). Storing chrominance components so interlaced enables FIFO that stores chrominance to have same structure as FIFO storing luminance (c. 10, ll. 8-9), and so creates symmetry. So, McGuinness teaches step of placing virtual memory page boundary across luminance chunk, virtual memory page boundary being associated with packetization scheme.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Rege to include placing virtual memory page boundary across luminance chunk, virtual memory page boundary associated with packetization scheme because McGuinness teaches reducing latency for reading encoded bitstream for video (c. 9, ll. 60-c. 10, ll. 9; c. 2, ll. 8-18). It would be obvious to modify Rege's method of selecting packetization scheme so it is used for reading encoded bitstream for video for reasons for Claim 4.

26. As per Claim 11, Rege does not teach step of placing virtual memory page boundary across chrominance chunk, virtual memory page boundary being associated with packetization scheme. According to Applicant's disclosure, virtual page boundary is placed to split left 2 words of each row. So, chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create symmetry that allows reduction of number of cases that need to be considered for packetization [0068]. McGuinness teaches interlacing the luminance Y and both chrominance Cr and Cb so all of the components can be retrieved in one word, reducing latency during rasterization without increasing time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (c. 10, ll. 26-30). Storing chrominance components so interlaced enables FIFO that stores chrominance to have same structure as the FIFO storing

luminance (c. 10, ll. 8-9), and so creates symmetry. So, McGuinness teaches step of placing virtual memory page boundary across chrominance chunk, virtual memory page boundary being associated with packetization scheme. This would be obvious for same reasons for Claim 10.

27. As per Claim 18, Rege does not explicitly teach plurality of data packets have 16 words. However, McGuinness teaches the plurality of data packets comprise 16 words (c. 9, ll. 7-11).

It would have been obvious to one of ordinary skill in the art to modify Rege so packets have 16 words because McGuinness teaches this is common size for packet (c. 9, ll. 7-11).

28. As per Claim 20, it is similar in scope to Claim 4, and so is rejected under same rationale.

29. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) and McGuinness (US006104416A) in view of Sorin (US006631164B1).

30. As per Claim 5, Rege and McGuinness are relied upon for teachings relative to Claim 4.

However, Rege and McGuinness do not teach step of determining location of read data further has receiving at least set of motion vectors pointing to reference pixel chunk. However, Sorin teaches step of determining location of read data further has receiving at least set of motion vectors pointing to reference pixel chunk (c. 6, ll. 31-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Rege and McGuinness's MPEG device (c. 4, ll. 60-62) so determining location of read data has receiving at least set of motion vectors pointing to reference pixel chunk because Sorin suggests motion vectors are needed in order to perform motion estimation to produce high quality MPEG digital video data of image (c. 1, ll. 30-39, 66-67; c. 2, ll. 1-2).

31. As per Claim 6, Rege and McGuinness do not teach determining first set of components associated with reference pixel chunk based on at least a set of motion vectors. But, Sorin

teaches step of determining first set of components associated with reference pixel chunk based on at least set of motion vectors (c. 6, ll. 31-45). This would be obvious for reasons for Claim 5.

32. As per Claim 7, Rege and McGuinness do not teach step of selecting packetization scheme further has combining part of luminance chunk and part of chrominance chunk into one of plurality of data packets to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages. However, Sorin teaches accessing blocks by combining them in a certain manner (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39). So, Sorin teaches step of selecting combining scheme further has combining part of luminance chunk and part of chrominance chunk into one of plurality of macroblocks to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Rege and McGuinness's MPEG device (c. 4, ll. 60-62) so step of selecting packetization scheme further has combining part of luminance chunk and part of chrominance chunk into one of plurality of data packets to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages because Sorin suggests this reduces number of pages changes needed to access MPEG digital video data of image (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39), which enables data to be accessed faster (c. 3, ll. 28-37).

33. As per Claim 8, Rege and McGuinness do not teach step of selecting packetization scheme has combining first part of luminance chunk and second part of luminance chunk into one of plurality of data packets to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages. However, Sorin teaches accessing blocks by combining them in certain manner (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39). So, Sorin teaches step of selecting

combining scheme further has combining first part of luminance chunk and second part of luminance chunk into one of plurality of macroblocks to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Rege and McGuinness's MPEG device (c. 4, ll. 60-62) so step of selecting packetization scheme further has combining first part of luminance chunk and second part of luminance chunk into one of plurality of data packets to be sent from memory when luminance chunk overlaps more than one of plurality of memory pages as suggested by Sorin. Sorin suggests typically, motion estimation calculations are performed on luminance values alone, for MPEG digital video data of image (c. 1, ll. 46-61). This also reduces number of pages changes needed to access MPEG digital video data of image (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39), which enables data to be accessed faster (c. 3, ll. 28-37).

34. As per Claim 9, Rege and McGuinness do not teach selecting packetization scheme has combining 1st part of chrominance chunk and 2nd part of chrominance chunk into one of plurality of data packets to be sent from memory when chrominance chunk overlaps more than one of plurality of memory pages. However, Sorin teaches accessing blocks by combining them in certain manner (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39). Sorin teaches step of selecting combining scheme further has combining first part of chrominance chunk and second part of chrominance chunk into one of plurality of macroblocks to be sent from memory when chrominance chunk overlaps more than one of the memory pages (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Rege and McGuinness's MPEG device (Col. 4, lines 60-62) so

step of selecting packetization scheme further has combining first part of chrominance chunk and second part of chrominance chunk into one of plurality of data packets to be sent from memory when chrominance chunk overlaps more than one of plurality of memory pages because Sorin suggests advantage of being able to combine blocks for greater transfer efficiency based on whether luminance data alone is needed, chrominance data alone is needed, or both luminance data and chrominance data are needed (c. 6, ll. 36-39). This also reduces number of pages changes needed to access MPEG digital video data of image (c. 4, ll. 64-c. 5, ll. 5; c. 6, ll. 36-39), which enables data to be accessed faster (c. 3, ll. 28-37).

35. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) in view of Levy (US005170251A).

Rege is relied upon for teachings relative to Claim 1. Rege teaches packet data is stored in array of pages 305, which are 512 bytes large. Packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (c. 6, ll. 12-22). Each of the pages has plurality of words (c. 6, ll. 60-65). So, Rege teaches packetization scheme selected maps packet data (first set of components) to selected ones of array of pages 305 containing plurality of words (second set of components). Claim 13 recites first set of components has data and second set of components has selected ones of plurality of words. So, Rege teaches packetization scheme selected maps first set of components (packet data) to second set of components (selected ones of plurality of words).

However, Rege does not teach selecting the packetization scheme by a table lookup. However, Levy describes selecting the packetization scheme by a table lookup (c. 2, ll. 20-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Rege to include selecting packetization scheme by table lookup as suggested by Levy. Speed gained by using lookup table can be significant, since retrieving value from memory is often faster than undergoing expensive computation, and this is well-known.

36. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) and Levy (US005170251A) in view of McGuinness (US006104416A).

Rege and Levy are relied upon for the teachings as discussed above relative to Claim 12.

However, Rege and Levy do not teach first set of components has read data corresponding to luminance chunk and chrominance chunk, and second set of components has selected ones of plurality of words. However, McGuinness teaches first set of components has read data corresponding to luminance chunk and chrominance chunk, and second set of components has selected ones of plurality of words (c. 9, ll. 55-59; c. 10, ll. 4-7).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Rege and Levy so first set of components has read data corresponding to luminance chunk and chrominance chunk, and second set of components has selected ones of plurality of words because McGuinness teaches this allows for interlacing of chrominance components in such a manner as to allow chrominance components to be retrieved in one word, reducing latency during rasterization, and because all of chrominance for one tile can still be retrieved in one burst the time to retrieve chrominance for decoding is not increased (c. 9, ll. 60-65). Storing chrominance components so interlaced enables FIFO that stores to chrominance to have same structure as FIFO storing luminance, so different structured FIFOs are not required (c. 10, ll. 8-17). This increases efficiency of retrieving encoded bitstreams for video

(c. 2, ll. 8-18). It would have been obvious to modify Rege's method of selecting packetization scheme so it is used for reading encoded bitstream for video for same reasons given for Claim 4.

37. Claims 21-23 and 28-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Artieri (US005579052A) in view of Rege (US005390299A).

38. As per Claim 21, Artieri teaches method for reassembling reference pixel data from plurality of data packets into luminance chunk and chrominance chunk (c. 18, ll. 21-37; c. 3, ll. 34-51), comprising receiving plurality of data packets, each data packet having portion of reference pixel chunk including luminance chunk and chrominance chunk; determining scheme used to output luminance and chrominance chunks in plurality of data packets based upon locations in memory of data; and unpacking plurality of data packets into reassembled luminance chunk and reassembled chrominance chunk based on scheme (c. 1, ll. 30-45; c. 3, ll. 34-51). Artieri teaches determining position in picture memory from which packets of data must be transferred. Instruction processor includes address register containing address at which read operation is carried out. After determining position, content of address register is modified. This modification may consist in incrementation (which amount to write or to read data at successive addresses in picture memory) or in more complex calculation (for example recursive calculation to extract picture line from sequence of macro-blocks) (c. 16, ll. 33-47). So, based on locations of read data, packets can be combined by reading data at successive addresses, or packets can be combined by more complex calculation, such as recursive calculation to extract picture line from sequence of macro-blocks. So, Artieri teaches selecting scheme based upon location in memory and then combining data into packets according to that scheme.

However, Artieri does not teach determining packetization scheme used to **packetize** luminance and chrominance chunks into plurality of data packets based upon locations in memory of data; unpacking based on packetization scheme. However, Rege teaches determining packetization scheme used to packetize data into plurality of data packets based upon locations in memory of data; unpacking based on packetization scheme (c. 6, ll. 60-68; c. 7, ll. 1-12, 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Artieri to include determining scheme used to packetize luminance and chrominance chunks into data packets based upon locations in memory of data; unpacking based on packetization scheme because Rege teaches if more than 1 page of data needs to be transferred, it can be transferred in 1 packet, so increasing transferring efficiency (c. 6, ll. 18-22).

39. As per Claim 22, Artieri teaches forming prediction blocks by arranging data packets unpacked with any data related to motion vectors (c. 1, ll. 36-45; c. 3, ll. 34-50), combining blocks with associated macroblocks to form reconstructed macroblock (c. 1, ll. 64-c. 2, ll. 3).

40. As per Claim 23, Artieri teaches writing reconstructed macroblock to memory (c. 7, ll. 47-50) having memory pages; selecting packetization scheme based on location of read data and on fitting read data into data packets; and assembling at least one read command for fetching read data from memory in accordance with packetization scheme selected (c. 16, ll. 32-47).

But, Artieri does not teach data packet contains data from more than one of plurality of memory pages. But, Rege teaches at least one data packet contains data from more than one of plurality of memory pages (c. 6, ll. 18-22). This would be obvious for reasons for Claim 21.

41. As per Claim 28, Artieri teaches system for decoding pictures in compressed video bit stream (c. 3, ll. 6-8; c. 6, ll. 33-34), having memory (15, Fig. 3; c. 6, ll. 37-41) having plurality of

memory pages (c. 18, ll. 21-30) storing reference pixel data (c. 7, ll. 52-67); address generator (24) coupled to memory for generating memory commands for fetching reference pixel data from memory; means for packing fetched reference pixel data into plurality of data packets according to specifications of memory commands (c. 16, ll. 32-47; c. 13, ll. 18-25); reference data assembly module (FIFOs) coupled to address generator for receiving from memory plurality of data packets (c. 6, ll. 45-48); and means for unpacking plurality of data packets and resassembling fetched reference pixel data into reassembled video bit stream (c. 1, ll. 36-45; c. 3, ll. 34-50). Artieri teaches determining position in picture memory from which packets of data must be transferred. Instruction processor includes address register containing address at which read operation is carried out. After determining position, content of address register is modified. Modification may consist in incrementation (which amount to write or to read data at successive addresses in picture memory) or in more complex calculation (for example recursive calculation to extract picture line from sequence of macro-blocks) (c. 16, ll. 33-47). So, based on locations of read data, packets can be combined by reading data at successive addresses, or packets can be combined by more complex calculation, such as recursive calculation to extract picture line from sequence of macro-blocks. So, Artieri teaches packing fetched reference pixel data into plurality of data packets according to the specifications of the memory commands.

But, Artieri doesn't teach data packet contains data from more than one of plurality of memory pages. But, Rege teaches at least one data packet contains data from more than one of plurality of memory pages (c. 6, ll. 18-22). This would be obvious for reasons for Claim 21.

42. As per Claim 29, Artieri teaches reference pixel data has luminance chunk and chrominance chunk (c. 1, ll. 30-45).

43. As per Claim 30, Artieri teaches memory commands have specification for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets (c. 16, ll. 32-47).

44. As per Claim 31, Artieri teaches reference data assembly module (FIFO) unpacks plurality of data packets to transform reference pixel data into a reassembled luminance chunk and a reassembled chrominance chunk (c. 18, ll. 31-37; c. 10, ll. 16-18).

45. As per Claim 32, Artieri teaches reference data assembly module has plurality of data buffers, each data buffer being configured to receive one of data packets (c. 9, ll. 45-48).

46. As per Claim 33, Artieri teaches reference data assembly module has additional module (14, Fig. 3) for reassembling reference pixel data based on set of motion vectors (c. 10, ll. 32-34; c. 10, ll. 52-65; c. 1, ll. 39-45) and packetization scheme used to form plurality of data packets (c. 11, ll. 26-34; c. 9, ll. 45-52).

But, Artieri does not teach table lookup used to form data packets. But, Levy teaches table lookup used to form plurality of data packets (c. 2, ll. 20-30), as discussed for Claim 12.

47. As per Claim 34, Artieri teaches reference data assembly module has plurality of data buffers for buffering a reassembled luminance chunk and reassembled chrominance chunk (c. 18, ll. 31-37; c. 10, ll. 16-18).

48. As per Claim 35, Artieri teaches variable length decoding module (10, Fig. 3) configured to extract set of motion vectors corresponding to macroblock in the compressed video bit stream (c. 7, ll. 10-15; c. 6, ll. 33-39).

49. As per Claim 36, Artieri teaches variable length decoding module (10, Fig. 3) sends the extracted set of motion vectors to the address generator (24) (c. 7, ll. 10-15).

50. As per Claim 37, Artieri teaches memory interface unit (instruction register) coupled to the memory (c. 13, ll. 59-64).

51. As per Claim 38, Artieri teaches the memory interface unit further comprises a memory queue for storing the generated memory commands from the address generator (c. 13, ll. 59-64).

52. As per Claim 39, Artieri teaches at least one of plurality of data packets includes reference pixel data from at least two of plurality of memory pages (c. 18, ll. 31-37) based on generated memory commands in the memory queue (c. 16, ll. 32-47; c. 13, ll. 59-64).

53. As per Claim 40, Artieri teaches memory interface unit (24, Fig. 5; c. 13, ll. 18-25) further has sequencer for forwarding generated memory commands to memory to obtain reference pixel data based on specifications (c. 16, ll. 32-47).

54. As per Claim 41, Artieri teaches memory interface unit (24) further has packet assembly unit (FIFO) for assembling plurality of data packets of reference pixel data obtained from memory (c. 6, ll. 45-51; c. 9, ll. 45-52).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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